IN THE CLAIMS

Please amend the claims as shown in the following detailed claim listing. The detailed claim listing is intended to reflect cancellation of claims 3, 5-6, 13-15, 20, 25-31, 33, 37, and 41; the amendment of previously pending claims 1, 4, 19, 32, 36, and 40; and the addition of new claims 46-51. The specific amendments to individual claims are detailed in the following detailed claim listing.

1. (Currently Amended) A substrate on which to mount an integrated circuit (IC) having a first dense formation of lands, the substrate comprising:

a second dense formation of lands on a surface thereof formed in a geometrical pattern to maximize the density of the second dense formation of lands, while constrained by the size of individual lands and by the width and spacing of substrate traces coupled to the lands,

wherein the second dense formation of lands is formed in a pattern comprising a combination of a face center rectangular pattern and a zigzag pattern having a plurality of zigzag rows ~~pattern from the group consisting of a zigzag pattern, a wave pattern, an undulating pattern, a vertical stack pattern, and any combination of a zigzag pattern, a wave pattern, an undulating pattern, and a vertical stack pattern~~.

2. (Previously Amended) The substrate recited in claim 1, wherein the maximum trace escape density equals the reciprocal of (Tw + Ts), and wherein Tw equals the width of the substrate traces and Ts equals the spacing between the substrate traces.

3. (Canceled)

4. (Currently Amended) The substrate recited in claim 1, ~~3,~~ wherein the plurality of zigzag rows are substantially parallel.

5-6. (Canceled)

7. (Previously Amended) An electronic package comprising:

an integrated circuit (IC) comprising a first plurality of lands on a surface thereof, including a first dense formation of lands;

a substrate comprising a second plurality of lands on a surface thereof, including a second dense formation of lands formed in an undulating pattern to maximize the density of the second dense formation of lands, while constrained by the size of the second dense formation of lands and by the width and spacing of substrate traces coupled to the second dense formation of lands; and

elements coupling the first plurality of lands to the second plurality of lands.

8. (Previously Amended) The electronic package recited in claim 7, wherein the maximum trace escape density equals the reciprocal of (Tw + Ts), and wherein Tw equals the width of the substrate traces and Ts equals the spacing between the substrate traces.

9. (Previously Amended) The electronic package recited in claim 7, wherein the second dense formation of lands is formed as a plurality of undulating rows at the periphery of the surface of the substrate.

10. (Previously Amended) The electronic package recited in claim 7, wherein the second dense formation of lands further comprises a face center rectangular pattern.

11. (Original) The electronic package recited in claim 7, wherein the IC is an unpackaged die.

12. (Original) The electronic package recited in claim 7, wherein the IC is a packaged die.

13-15. (Cancelled)

16. (Previously Amended) A data processing system comprising:

a bus coupling components in the data processing system;

a display coupled to the bus;

external memory coupled to the bus; and

a processor coupled to the bus and including at least one electronic package comprising:

an integrated circuit (IC) comprising a first plurality of lands on a surface thereof, including a first dense formation of lands;

a substrate comprising a second plurality of lands on a surface thereof, including a second dense formation of lands formed in an undulating pattern to maximize the density of the second dense formation of lands, while constrained by the size of the second dense formation of lands and by the width and spacing of substrate traces coupled to the lands; and

elements coupling the first plurality of lands to the second plurality of lands.

17. (Previously Amended) The data processing system recited in claim 16, wherein the second dense formation of lands is formed as a plurality of undulating rows at the periphery of the surface of the substrate.

18. (Original) The data processing system recited in claim 16, wherein the IC is an unpackaged die.

19. (Currently Amended) A method comprising:

forming on a substrate surface a plurality of traces, the traces having at least a predetermined width and a predetermined spacing from one another; and

forming within a die-bonding area on the substrate surface a plurality of lands, each coupled to a corresponding one of the plurality of traces, and each having at least a predetermined size, the plurality of traces escaping the die-bonding area, the plurality of lands being formed in at least one geometrical pattern that maximizes the trace escape density while constrained by the land size and by the width and spacing of the traces, wherein the at least one geometrical pattern comprises a vertical stack pattern having at least three or more lands in a vertical stack, wherein the maximum trace escape density equals the reciprocal of (Tw + Ts), and wherein Tw equals the width of the traces and Ts equals the spacing between the traces.

20. (Canceled)

21. (Previously Amended) The method recited in claim 19, wherein the plurality of lands are formed as a plurality of vertical stack patterns at the periphery of the surface of the substrate.

22. (Previously Amended) The method recited in claim 21, wherein the plurality of vertical stack patterns each comprise at least three lands, and wherein the substrate traces coupled to corresponding lands in each vertical stack are all located on the same side of the vertical stack.

23. (Previously Amended) The method recited in claim 19, wherein the at least one geometrical pattern further comprises an undulating pattern.

24. (Previously Amended) The method recited in claim 19, wherein the at least one geometrical pattern further comprises a face center rectangular pattern.

25-31. (Cancelled)

32. (Currently Amended) A method comprising:

forming lands within a die-bonding area on a substrate surface in a geometrical pattern to maximize the trace escape density of traces coupled to the lands and escaping the die-bonding area on the substrate surface while constrained by the land size and by the width and spacing of the traces, wherein the lands are formed in a vertical stack pattern having at least three or more lands in a vertical stack, wherein the maximum trace escape density equals the reciprocal of (Tw + Ts), and wherein Tw equals the width of the traces and Ts equals the spacing between the traces; and

coupling lands on an integrated circuit (IC) to corresponding lands on the substrate surface.

33. (Canceled)

34. (Original) The method recited in claim 32, wherein the IC is an unpackaged die.

35. (Original) The method recited in claim 32, wherein the IC is a packaged die.

36. (Currently Amended) A substrate having a die-bonding area on which to mount an integrated circuit (IC) having a first dense formation of lands, the substrate comprising:

a second dense formation of lands on a surface thereof and within the die-bonding area, each land having coupled thereto a substrate trace escaping the die-bonding area;

wherein the second dense formation of lands is formed in an undulating pattern, wherein the maximum trace escape density equals the reciprocal of (Tw + Ts), and wherein Tw equals the width of the traces and Ts equals the spacing between the traces.

37. (Canceled)

38. (Previously Added) The substrate recited in claim 36, wherein the second dense formation of lands comprises a plurality of undulating rows at the periphery of the surface of the substrate.

39. (Previously Added) The substrate recited in claim 36, wherein the second dense formation of lands further comprises a face center rectangular pattern.

40. (Currently Amended) A substrate having a die-bonding area on which to mount an integrated circuit (IC) having a first dense formation of lands, the substrate comprising:

a second dense formation of lands on a surface thereof, each land having coupled thereto a corresponding substrate trace escaping the die-bonding area;

wherein the second dense formation of lands is formed in a vertical stack pattern having at least one group of three or more lands in a vertical stack; ~~and~~

wherein the substrate traces coupled to corresponding lands in a vertical stack are all located on the same side of the vertical stack; and

wherein the maximum trace escape density equals the reciprocal of (Tw + Ts), and wherein Tw equals the width of the traces and Ts equals the spacing between the traces.

41. (Canceled)

42. (Previously Added) The substrate recited in claim 40, wherein the second dense formation of lands comprises a plurality of vertical stacks at the periphery of the surface of the substrate.

43. (Previously Added) The substrate recited in claim 40, wherein the second dense formation of lands further comprises a face center rectangular pattern.

44. (Previously Added) The method recited in claim 32, wherein the lands are formed as a plurality of vertical stack patterns at the periphery of the surface of the substrate.

45. (Previously Added) The method recited in claim 44, wherein the plurality of vertical stack patterns each comprise at least three lands, and wherein the traces coupled to corresponding lands in each vertical stack are all located on the same side of the vertical stack.

46. (New) A substrate on which to mount an integrated circuit (IC) having a first dense formation of lands, the substrate comprising:

a second dense formation of lands on a surface thereof formed in a geometrical pattern to maximize the density of the second dense formation of lands, while constrained by the size of individual lands and by the width and spacing of substrate traces coupled to the lands,

wherein the second dense formation of lands is formed in a pattern comprising a combination of a face center rectangular pattern and an undulating pattern.

47. (New) The substrate recited in claim 46, wherein the maximum trace escape density equals the reciprocal of (Tw + Ts), and wherein Tw equals the width of the substrate traces and Ts equals the spacing between the substrate traces.

48. (New) The substrate recited in claim 46, wherein the undulating pattern comprises a plurality of rows.

49. (New) A substrate on which to mount an integrated circuit (IC) having a first dense formation of lands, the substrate comprising:

a second dense formation of lands on a surface thereof formed in a geometrical pattern to maximize the density of the second dense formation of lands, while constrained by the size of individual lands and by the width and spacing of substrate traces coupled to the lands,

wherein the second dense formation of lands is formed in a pattern comprising a combination of a face center rectangular pattern and a wave pattern.

50. (New) The substrate recited in claim 49, wherein the maximum trace escape density equals the reciprocal of (Tw + Ts), and wherein Tw equals the width of the substrate traces and Ts equals the spacing between the substrate traces.

51. (New) The substrate recited in claim 49, wherein the wave pattern comprises a plurality of rows.